IN THE ABSTRACT

Please amend the Abstract as follows.

ABSTRACT

~~Disclosed is a semiconductor integrated circuit device constructed of MOSFETs in which there is attained a harmony between increase in consumption power due to a leakage current and operating speed of the MOSFETs in a suitable manner, and among a plurality of signal paths in the semiconductor integrated circuit device, a path which has a margin in delay is constructed with MOSFETs each with a high threshold voltage, while a path which has no margin in delay is constructed with MOSFETs each with a low threshold voltage which has a large leakage current but a high operating speed, in light of a delay with which a signal is transmitted along a signal path~~ This invention provides a storage medium on which there is stored a cell library to design a semiconductor integrated circuit to satisfy low power consumption and high speed operation and a design method using the cell library. The cell library is registered with at least two kinds of cells which are different in delay and power consumption while having the same function and the same shape. To satisfy the specification of the semiconductor integrated circuit, one cell is selected from at least two kinds of cells of the cell library.